การสร้างวงจรนับอย่างง่าย

Lead-free Green

NE555

PRECISION TIMER

Description

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

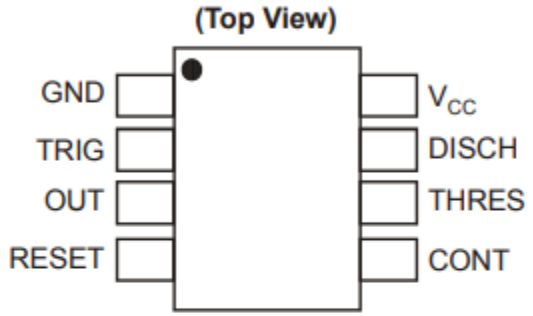
The threshold and trigger levels normally are two-thirds and one-third, respectively, of V_{CC}. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set, and the output goes high. If the trigger input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset, and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200mA. Operation is specified for supplies of 5V to 15V. With a 5-V supply, output levels are compatible with TTL inputs.

Features

- Timing from microseconds to hours
- Astable or monostable operation
- Adjustable duty cycle
- TTL compatible output can source or sink up to 200mA
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen- and Antimony-Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative.**
  https://www.diodes.com/quality/product-definitions/

Pin Assignments

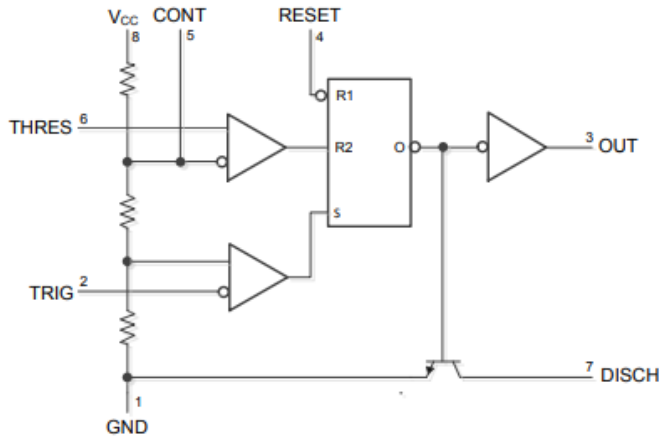


SO-8

Pin Descriptions

Pin Name	Pin Number	Description
GND	1	Ground
TRIG	2	Trigger set 1/3V_{CC}
OUT	3	Timer output
RESET	4	Reset active low
CONT	5	External adjustment of internal threshold and trigger voltages
THRES	6	Threshold set to 2/3 V_{CC}
DISCH	7	Low impedance discharge path
V_{CC}	8	Chip supply voltage

Functional Block Diagram



RESET can override TRIG, which can override THRESH

Functional Table

RESET	Nominal Trigger Voltage	Threshold Voltage	Output	Discharge Switch
Low	Irrelevant	Irrelevant	Low	On
High	<1/3V_{CC}	Irrelevant	High	Off
High	>1/3V_{CC}	>2/3V_{CC}	Low	On
High	>1/3V_{CC}	<2/3V_{CC}	As previously established	

FAIRCHILD SEMICONDUCTOR™

August 1986
Revised July 2001

DM7408
Quad 2-Input AND Gates

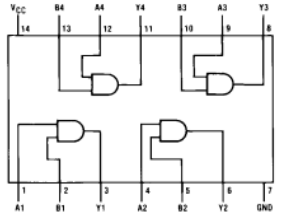
General Description

This device contains four independent gates each of which performs the logic AND function.

Ordering Code:

Order Number	Package Number	Package Description
DM7408N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram



Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = HIGH Logic Level
L = LOW Logic Level

DM7408 Quad 2-Input AND Gates

National Semiconductor

January 1988

MM54HC390/MM74HC390
Dual 4-Bit Decade Counter
MM54HC393/MM74HC393
Dual 4-Bit Binary Counter

General Description

These counter circuits contain independent ripple carry counters and utilize advanced silicon-gate CMOS technology. The MM54HC390/MM74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter. The MM54HC393/MM74HC393 contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

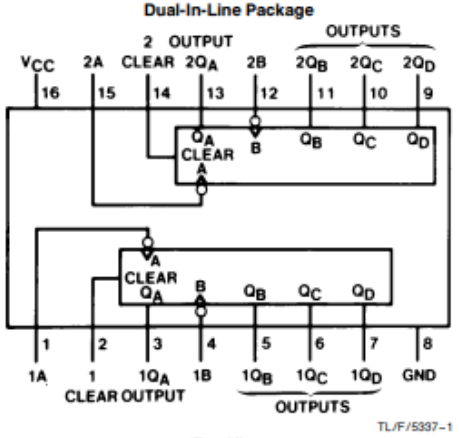
Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. These counters are functionally as well as pin equivalent to the 54LS390/74LS390 and the 54LS393/74LS393, respectively. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

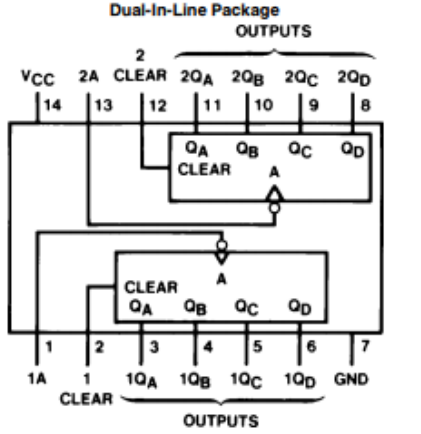


TL/F/5337–1

Top View

Order Number MM54HC390 or MM74HC390

Dual-In-Line Package

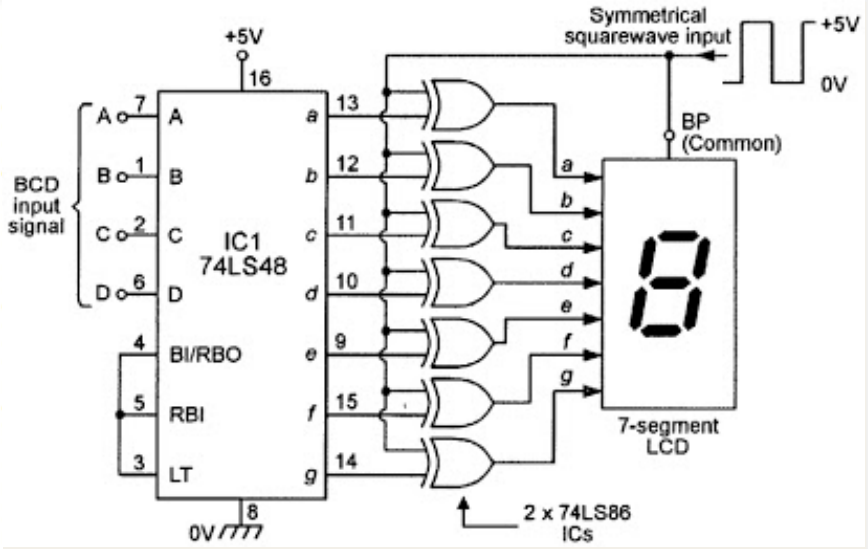


TL/F/5337–2

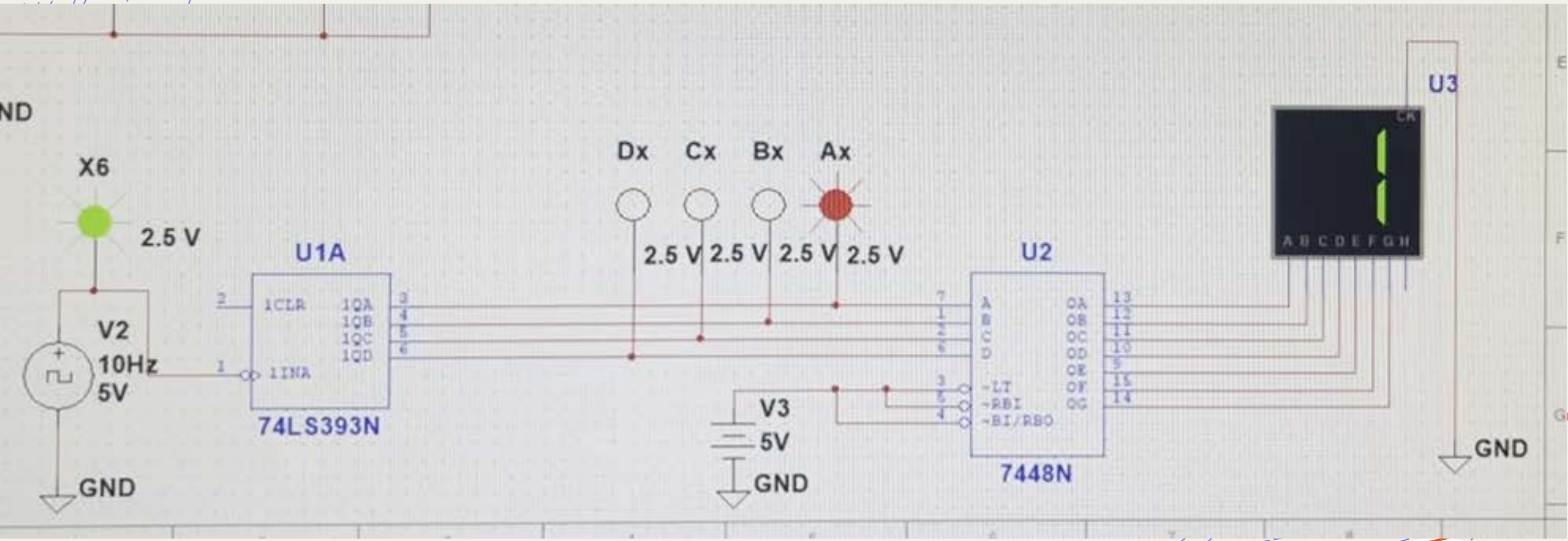
Top View

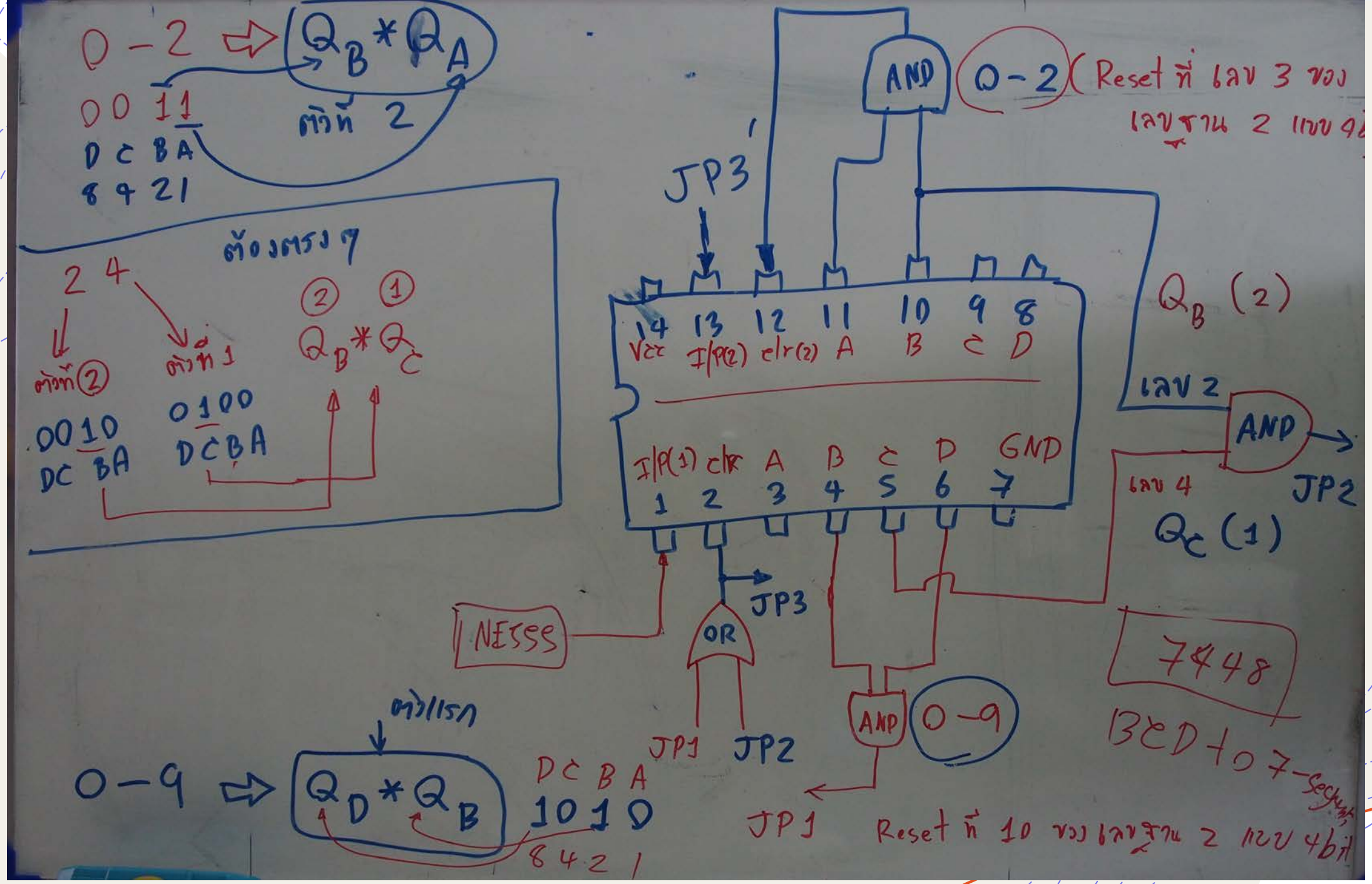
Order Number MM54HC393 or MM74HC393

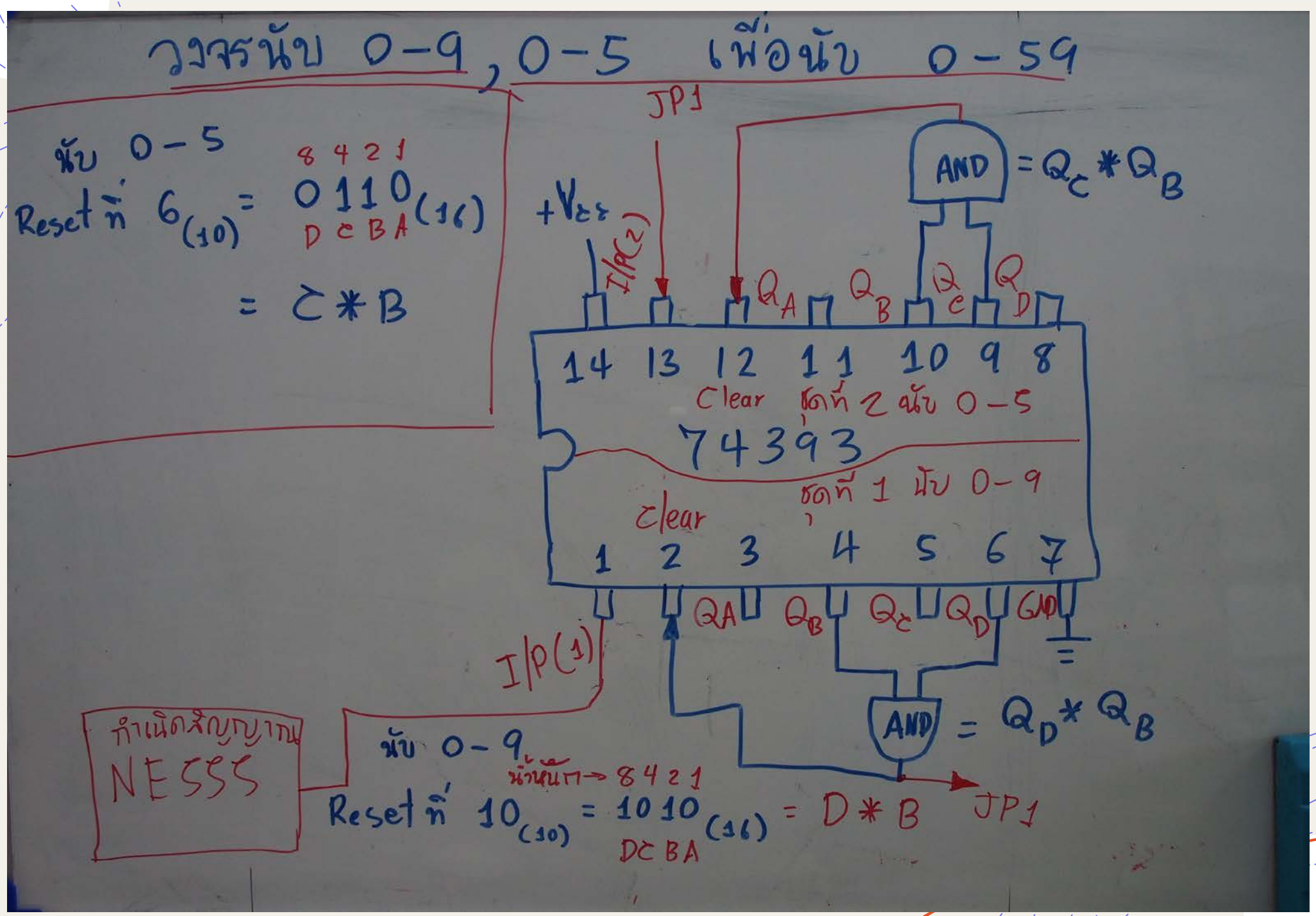
RRD-B30M105/Printed in U. S. A.

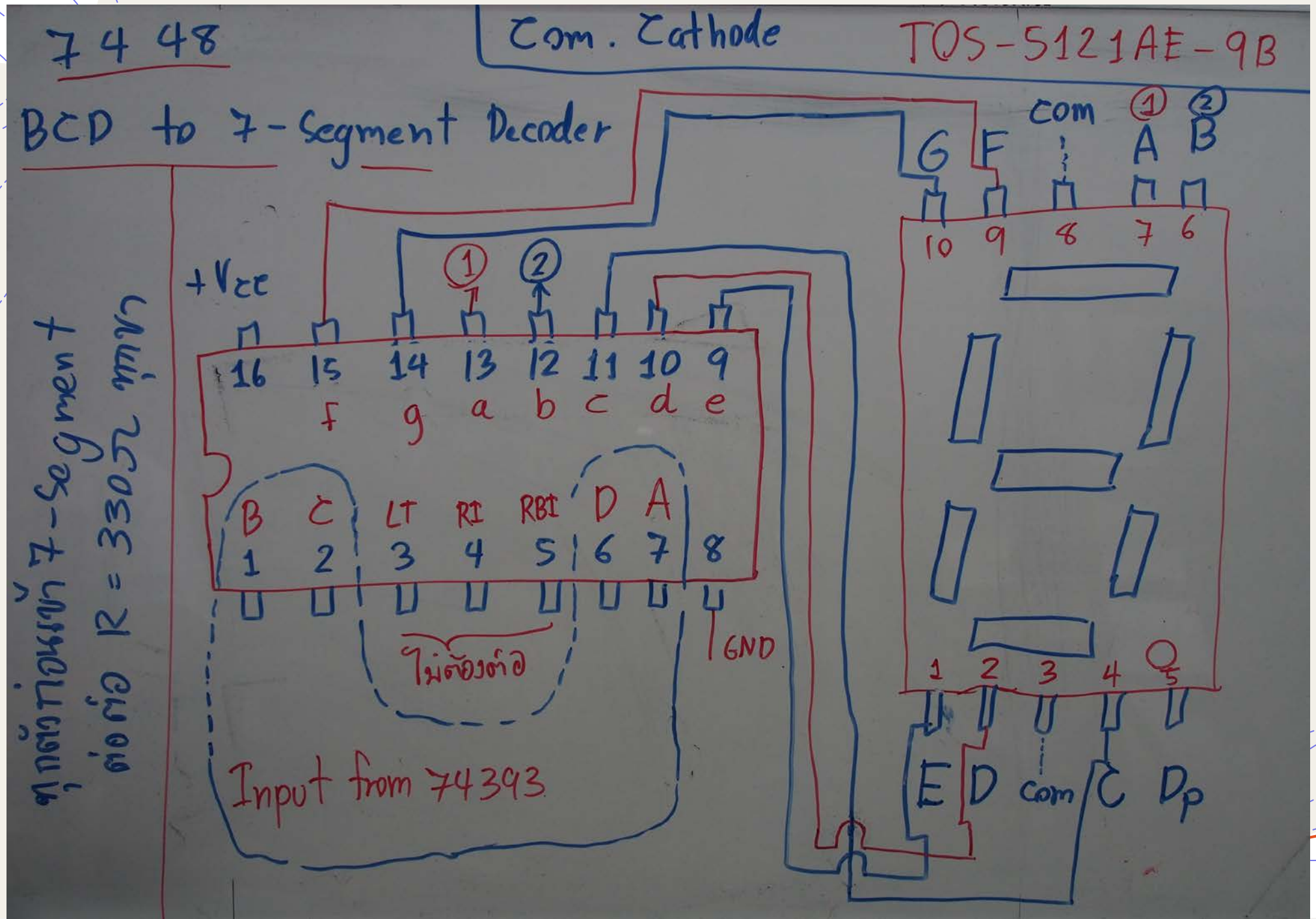


Simulate by Multisim




0 - 2
$Q_B * Q_A$
00 11
DCBA
8421
ตัวที่ 2
ต้องตรง 7
24
ตัวที่ 2
ตัวที่ 1
0010
DCBA
0100
DCBA
$Q_B * Q_C$
AND
0 - 2
Reset ที่ เลข 3 ของ
เลขฐาน 2 แบบ 4
JP3
14 13 12 11 10 9 8
Vcc I/P(2) clr(2) A B C D
I/P(1) clr A B C D GND
1 2 3 4 5 6 7
Q_B (2)
เลข 2
AND
เลข 4
Q_C (1)
JP2
NE555
OR
JP3
7448
BCD to 7-Segment
ตัวแรก
0 - 9
$Q_D * Q_B$
DCBA
1010
8421
JP1
JP2
AND
0 - 9
JP1
Reset ที่ 10 ของเลขฐาน 2 แบบ 4bit


วงจรนับ 0-9, 0-5 เพื่อนับ 0-59
นับ 0-5
8 4 2 1
Reset ที่ 6(10) = 0 1 1 0 (16)
D C B A
= C * B
JP1
+Vcc
I/P(2)
AND
= QC * QB
QA QB QC QD
14 13 12 11 10 9 8
Clear ชุดที่ 2 นับ 0-5
74393
ชุดที่ 1 นับ 0-9
clear
1 2 3 4 5 6 7
QA QB QC QD GND
I/P(1)
AND
= QD * QB
กำเนิดสัญญาณ
NE555
นับ 0-9
น้ำหนัก → 8 4 2 1
Reset ที่ 10(10) = 1 0 1 0 (16)
D C B A
= D * B
JP1


7448
BCD to 7-Segment Decoder
Com. Cathode
TOS-5121AE-9B
+Vcc
16 15 14 13 12 11 10 9
f g a b c d e
B C LT RI RBI D A
1 2 3 4 5 6 7 8
GND
ไม่ต้องต่อ
Input from 74393
ต่อตัวต้านทาน 7-Segment ตัวละ R = 330Ω ทุกขา
com
G F A B
10 9 8 7 6
1 2 3 4 5
E D com C Dp